HIGH FREQUENCY PERFORMANCE OF IMPLANTED Si-MOSFETs

C. Tsironis, U. Niggebrügge

Institute of Semiconductor Electronics
Technical University Aachen
Templergraben 55, 51 Aachen, F.R.G.

ABSTRACT

Silicon MOSFETs with a 0.8 µm long channel, made by conventional technology and optimized for microwave applications, have noise figure of 3.5 dB at 4 GHz and f_{max} of 10 to 12 GHz. The noise and RF small signal performance are very slightly affected by channel ion implantation, used to shift the threshold voltage to positive values. The RF equivalent circuit analysis indicates negligible parasitic lead resistances but high feedback capacitance.

Introduction

Si-MOSFETs are primarily used in digital circuits and frequencies below 1 - 2 GHz. Parasitics caused by the non satisfactory isolation of the substrate material combined with the lower mobility in comparison with GaAs limit the high frequency performance of these devices. By appropriate design of the device geometry and optimization of the technology, n-channel Si-MOSFETs with usable characteristics up to the G-band have been realized [1]. It has been shown that the use of ion implantation to overcome two dimensional effects like negative threshold voltages and punch through has no essential effect on RF device behaviour though enabling normally OFF FETs. A numerical simulation of the small signal behaviour indicates that f_{max} values up to 15 GHz are possible by a slightly modified geometry. Further advantages of the Si-MOSFETs (especially in comparison with GaAs devices) are the high uniformity in DC and RF characteristics and the high reliability resulting from the mostly conventional technology. The absence of low frequency trapping effects causes a high time constancy of the device characteristics.

Device fabrication, DC-characteristics

A cross section of the MOSFET structure is given on fig. 1. The used technology consists of phosphorous diffusion for source and drain contact-doping, thermal dry

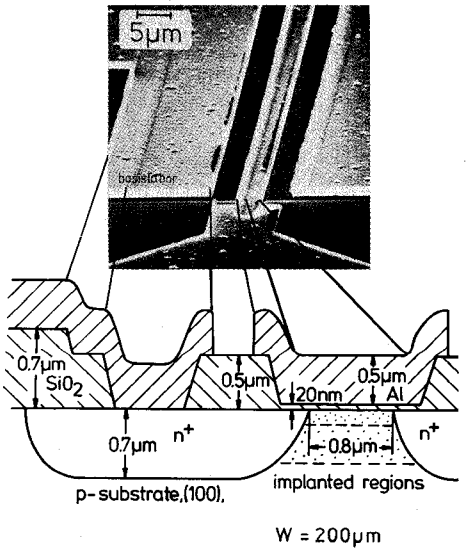

Fig. 1: SEM photo and schematic cross section of the inner region of the Si-MOSFETs.

oxidation for gate and masking oxides and optical projection printing. The demands for good high frequency behaviour could be fulfilled by the following parameters: Short channel length of ca. 0.8 µm (estimated from the mask dimensions and one dimensional analysis of the diffusion depth) for small transit time and thin gate oxide of 20 nm for high transconductance; gate-drain overlap of 0.4 µm, thick field oxide of 0.7 µm and low-doped substrate of 1.2×10^{15} cm^{-3} were used to keep parasitic capacitances small; the drain and source metallization areas (including bonding pads) were kept as small as possible ($\simeq$ 0.01 mm^2) to avoid pad parasitic capacitances; thick aluminium gate evaporation permitted a very low gate resistance; the device width was 200 µm.
The negative threshold voltage (-2 V) of the devices on the low doped substrate (FM 36) could be shifted to positive values (0.2 V) by single ion implantation, the energy and dose being 30 keV and 10^{12} cm^{-2} resp. (FM 37). A deeper boron implantation (110 keV, 2-8 x 10^{11} cm^{-2}, FM 38, 39, 40) increased the punch-through voltage to $V_{DS} \geq 5$ V. Output DC characteristics of the fabricated Si-MOSFETs are shown on fig. 2.

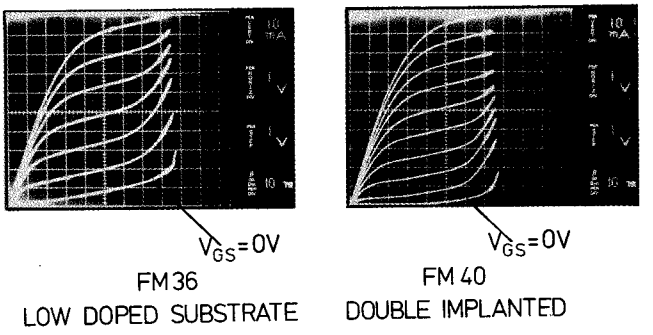

Fig. 2: DC characteristics of Si-MOSFETs.

RF characteristics

Maximum frequency of oscillation

The RF behaviour of the MOSFETs was analyzed by means of s-parameter measurements up to 14 GHz [2]. Typical MAG-values calculated from measured s-parameters are shown on fig. 3, where also the influence of a high doped substrate and local ion implantation in the low doped substrate is to be seen. The local peak at f = 8-9 GHz is possibly due to internal feedback in the MOSFETs since, as will be shown later, the feedback capacitance is still high. Using e-beam lithography a decrease of C_{gd} by a factor of 3 or 5 will be possible by avoiding overlap of drain and gate and, inspite of increase of the drain lead resistance, a f_{max} of 14-15 GHz is achievable for the present MOSFET structure, as calculations on the basis of the equivalent circuit of fig. 4 have shown.

Equivalent circuit

Using digital computer optimization techniques and starting from s-parameters at 10 frequencies between 1 and 12 GHz we determined an equivalent circuit for the

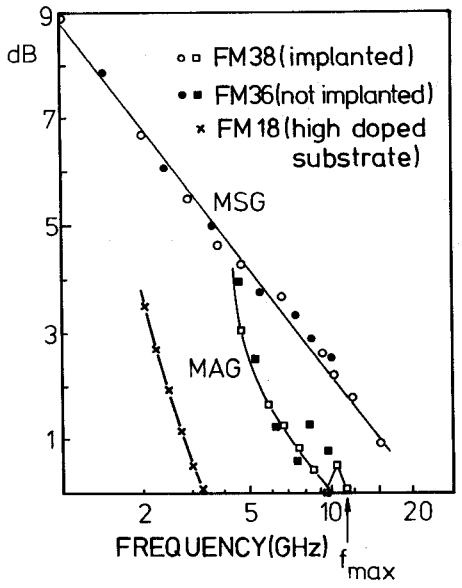

Fig. 3: MAG values of three types of Si-MOSFETs.

MOSFETs given on fig. 4. Special effort was spent to simulate the influence of the substrate contact, connected by bond wires with source, as the series resonant circuit between drain and source through substrate shows.
The values of the circuit elements differ slightly between implanted and not implanted devices but the principal structure remains, also the negligible source gate and drain lead resistances caused by the gate overlap over source and drain. The feedback capacitance C_{gd} in all analyzed MOSFET types is of the same order of magnitude (corresponding to approx. 10 times the feedback capacitance of a Si-MESFET with comparable geometry [3]).

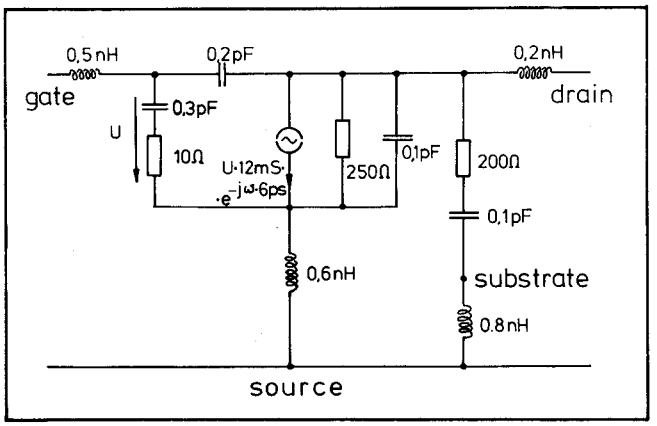

Fig. 4: Equivalent circuit of a Si-MOSFET (FM 38); the substrate is connected to source.

The achieved agreement between measured and simulated s-parameters by the equivalent circuit of fig. 4 is given on fig. 5 for an implanted MOSFET. The comparison between the measured and calculated S_{22} and S_{12} values indicates the obtained good simulation of the output device circuit.

Noise behaviour

The noise behaviour of the MOSFETs was experimentally investigated in the frequency region between 2 and 6 GHz, since at higher frequencies the gain available from the devices is poor. The optimum noise figure is given on fig. 6 for two different MOSFET types and two substrate temperatures to determine the origin of the excess noise at higher drain voltages (see also fig. 8).

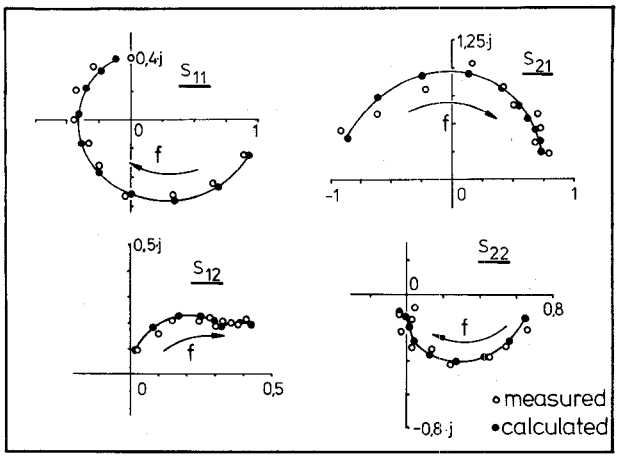

Fig. 5: Comparison between measured and calculated s-parameters of Si-MOSFETs; FM38, f= 1-12 GHz

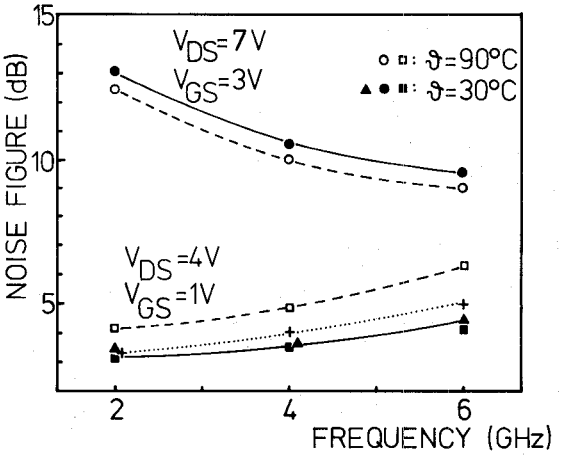

Fig. 6: Optimum noise figure of Si-MOSFETs.
▲: FM 40 (double implanted), V_{DS}=4V, V_{GS}=4V.
■ □ ● ○: FM 36 (not implanted)
+ Si-MESFET (after [3]).
ϑ: Chip temperature.

As the curves at ϑ = 90°C indicate avalanche noise affect the device noise figure at V_{DS} = 7 V, with an avalanche frequency below the measuring frequency region. Ion implanted MOSFETs have slightly higher noise figures (fig. 6) but the useful bias region is higher, as can be seen on fig. 7, so the implanted devices will be less bias-

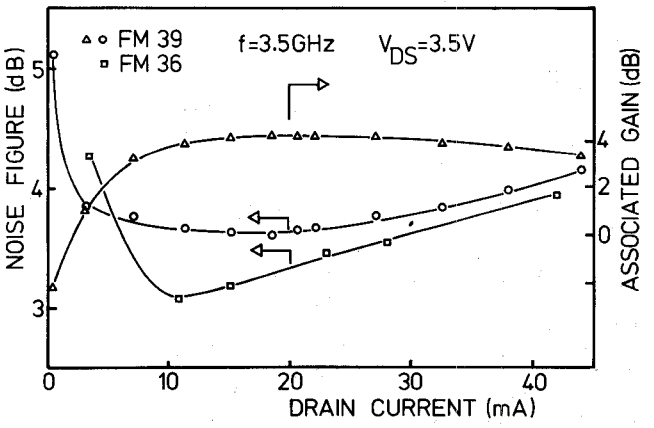

Fig. 7: Noise figure and associated gain of Si-MOSFETs as a function of drain current.

point sensitive in amplifier applications. The Si-MOSFETs are less linear concerning the drain than the gate voltage. This is valid for gain and for noise figure (fig.8).

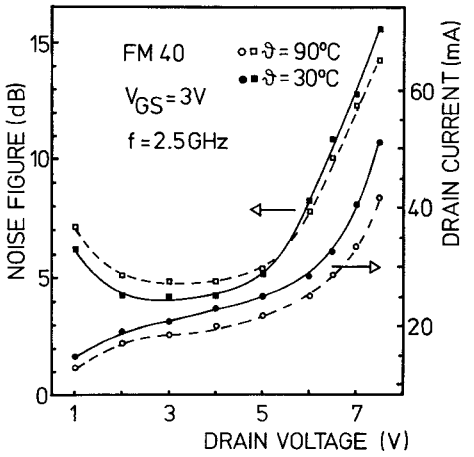

Fig. 8: Noise figure and drain current of a double implanted Si-MOSFET as a function of drain voltage for two chip temperatures ϑ .

Fig. 8 also shows the beginning of avalanche breakdown at 5 V, limiting also this way the available power from the devices although the MOSFETs withstand drain voltages up to 12 V without any change in DC and RF characteristics.

Large signal behaviour

Measurements of the forward voltage gain $|S_{21}|$ at 1 GHz show a high linearity as a function of gate bias with a 1 dB compression point between gate voltages of 2 and 9 V and a medium linearity as a function of drain bias with the 1 dB compression point between drain voltages of 2 and 6 V. The output power as a function of the input power is given in fig. 9.

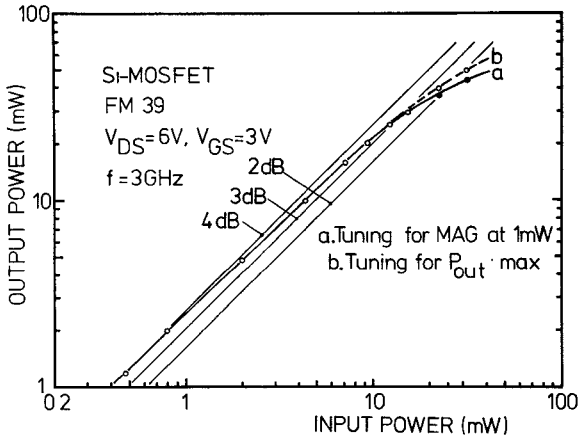

Fig. 9: Power saturation characteristics of Si-MOSFETs.

The 1 dB compression point is at P_{out} = 30 mW and 4 dB gain for a 200 µm wide device. By appropriate tuning of the output circuit the output power can be increased as fig. 9b shows. The power added efficiency η_{add} is here ≃ 10 %. The saturation power reaches here 100 mW for the device of fig. 9.

Large signal time domain analysis of the MOSFETs, important for digital applications, showed a pulse sharpening effect causing the output pulse rise time to be 48 ps and smaller than the input pulse rise time being 56ps [4] . The delay time for a single device was 46 ps. For the application in integrated logic circuits the channel width of the device shown is too large, a width of 20 µm should be needed. In this case however the parasitics will have more disadvantageous influence on device pulse response than on a device with a 200 µm wide channel.

Conclusion

Short channel silicon MOSFETs have been shown to be useful up to the G-band. The noise behaviour is slightly better than that of 1 µm silicon MESFETs reported so far. Ion implantation of the channel region for realization of normally OFF FETs with high punch through voltage does not affect essentially the RF small signal, noise and switching behaviour.

Acknowledgement

The authors wish to acknowledge Prof. Dr. H. Beneking and Prof. Dr. P. Balk for their interest in this work. The work has been supported by the SFB-56 "Festkörperelektronik".

References

[1] U. Niggebrügge et al., "Implanted Si-MOSFETs for high speed applications", Electronics Letters 14, No. 21, 690 (1978).

[2] C. Tsironis and R. Stahlmann, "High frequency performance and equivalent circuit of implanted n-channel Si-MOSFETs", 5th European Spec. Workshop on Active Semicond. Devices, Venice, Oct. 1978.

[3] W. Bächtold, P. Wolf, "An improved microwave silicon MESFET", Sol. St. Electr. 14, 783 (1971).

[4] W. Filensky, H. J. Klein and H. Beneking, "The GaAs MESFET as a Pulse Regenerator Amplifier and Laser Modulator in the Gbit/s Range", IEEE SC 12, 276, 709 (1977).